## APPENDIX

Claims 1 and 2 now read as follows.

1. (Amended) A semiconductor device comprising:

a first region where first transistors each having a first gate oxide film of a first thickness is formed;

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a second region, adjacent to the first region, where second transistors each having a second gate oxide film of a second thickness are formed;

trench isolation patterns formed selectively within said first and second regions and extending continuously in a first direction; and

a dummy region having a plurality of dummy trench isolation patterns located between said first and said second regions, wherein the dummy trench isolation patterns comprise a pattern which constitutes a positioning mark and extends in a second direction different from the first direction.

2. (Amended) A semiconductor device according to Claim 1, wherein said semiconductor device comprises a memory cell region in which memory cell transistors are formed and a peripheral circuit region in which a peripheral circuit for controlling the operation of said memory cell transistors is formed and wherein said first region includes said memory cell region and said second region includes said peripheral circuit region, wherein the first and second regions are arranged in the first direction and the dummy region extends in the first direction along the first and second regions.

Claim 3 has been cancelled.

Please add new claim 11.

11. (New) The semiconductor device according to Claim 1, wherein the pattern of the dummy trench isolation extends in a vertical direction with respect to the first direction.